

Prolonging 3D NAND SSD Lifetime via Read Latency Relaxation

Extended Abstract

Chun-Yi Liu¹, Yunju Lee¹, Myoungsoo Jung², Mahmut Taylan Kandemir¹, Wonil Choi¹
The Pennsylvania State University¹, KAIST²

1. Motivation

What is the problem your work attacks?

Many existing SSD-related works focus exclusively on write disturbances and retention errors [10, 11, 5, 12, 9, 2, 4]. In contrast, the attacked problem in this paper is the "read disturbance induced lifetime and performance issues" on state-of-the-art high-density 3D flash SSDs. Specifically, due to ultra-high-density of 3D flash, the read disturbances while performing reads become much severer than ever before. Unfortunately, it is difficult for the SSDs to solve or hide such undesired disturbance-induced issues through only SSD firmware or 3D flash-cell improvements. To address this problem, we propose and experimentally evaluate an *application/SSD co-design* approach, which can utilize application-specific performance requirements to reduce the read-induced SSD lifetime consumption and retain application-expected performance.

Why is it an important problem?

The markets keep demanding cheaper (price per GB) storage media with a decent random read performance. 3D NAND flash is a promising storage media, which possesses ultra-high density with great random read performance. However, 3D flash density-improving techniques, such as stacking more number of flash layers, can inevitably cause disturbance-induced lifetime/performance problems. Currently, the density of 3D NAND flash can keep increasing with no foreseen technical difficulties. However, the lifetime/performance problems caused by the read disturbance can prevent the density from further increasing. As a result, to make a higher density storage system, these problems have to be solved; but, firmware-level approaches alone can not achieve that. Therefore, this paper proposes an application/SSD co-design-based approach to address such problem.

2. Limitations of the State of the Art

What is the state of the art?

The targeted read-disturbance problem is typically addressed by improving the 3D flash cells or adopting a better SSD firmware management. In reality, manufacturing new types of 3D flash cells is a very time-consuming process; as a result, firmware-level solutions are more popular in practice.

What are its limits?

Firmware-level solutions include two techniques: (1) read disturbance characterization between 3D flash cells and (2) rewriting the read-disturbed data to eliminate them. The first technique collects the characterized data on a flash cell level to predict better read reference voltages to correctly read the dis-

turbed data with potentially-prolonged read latencies. On the other hand, the second technique eliminates the disturbed data by reading the disturbed data, correcting them, and rewriting them; as a result, the erroneous data are eliminated. However, additional rewrites have to be performed to the 3D flash.

In our SSD-level characterizations, we can observe that both techniques are adopted by the SSDs. For example, SSD-A/-B/-C/-D/-E/-F/-G/-H suffer from a large amount of the read-disturbance-induced rewrites. In contrast, SSD-I/-J suffer from the prolonged read latencies, which can degrade the overall read performance. Hence, 3D SSDs need a better approach to address such disturbance-induced problems.

3. Key Insights

What are the one or two key new insights in this paper?

- Our extensive SSD-level characterizations show that 3D SSDs suffer from either performance or lifetime degradation under a large amount of reads owing to the severe 3D flash read disturbance.
- Our proposed read latency relaxation uses "hint commands" to inform 3D SSDs about the application-desired read performance; as a result, the SSDs can reduce the read-induced rewrites without violating the application expected performance.

How does it advance the state of the art?

The state-of-the-art SSD works (from both academia and industry) are based upon the idea that these disturbance-induced issues should be and can be solved only by SSDs itself. However, as shown by our extensive characterization on state-of-the-art SSDs, SSD internal disturbance mitigations have limited capability to hide or mitigate the disturbance-induced performance/lifetime problems due to increasing severe read disturbance. Hence, in this paper, we propose to use the "hint commands" sent from hosts to 3D SSDs to assist SSDs to address the read disturbance-induced problems. Consequently, SSDs equipped with our proposal can reduce the disturbance-induced rewrites without degrading the application expected performance.

What makes it more effective than past approaches?

The reason that our proposal can be more effective is that we provide the application-desired performance (via the hint commands) from hosts to SSDs. Hence, the SSDs can schedule or postpone the rewrites to future points in time to strike a balance between SSD lifetime and performance.

4. Main Artifacts

What are the key artifacts?

- We present a long-period measurement methodology to test SSD lifetime and performance under a large amount of data. Specifically, we imposed low-throughput random read workloads to the tested SSDs to observe the changes in lifetime and performance for at least half-year period. This long-period approach helps us discover the aspects that cannot be observed from traditional short-period performance benchmarking.
- We propose a "hint command mechanism" to be used on host side to send additional information to inform the SSDs about the application-desired performance. As a result, the SSDs can in turn reduce the read-induced rewrites without degrading the application performance.

How were your artifacts implemented and evaluated?

For the first artifact, the long-period methodology can be implemented by fio [1] storage benchmark and the corresponding scripts. We are happy to release the testing scripts and the collected raw data after the paper gets published. For the second artifact, we use FEMU [7], an SSD emulation platform with both a (Linux) host system and an SSD emulator. This platform allows us to modify the host applications and SSD internal management to evaluate our proposal.

5. Key Results and Contributions

What are the most important one or two empirical or theoretical results of this approach?

- From our extensive lifetime-impact characterization on a large amount of reads, we observe that some SSDs rewrite the data being read 40 times to eliminate all read-induced performance problem. And, from our extensive latency-impact characterization on a large amount of reads, it is observed that the ratio of long reads (over $400\mu s$) can increase from 0.02% to 7.7%, which can greatly degrade the performance.
- By adopting our read latency relaxation proposal, the tested file-server application can reduce about 56% spent-lifetime caused by read-induced rewrites with only 2% performance overhead.

What are the contributions that this paper makes to the state of the art?

- We propose a long-period measurement methodology to quantify the lifetime and latency impacts under a large amount of reads. Our methodology helps us discover missing aspects of the current 3D high-density SSDs.
- We present some discoveries on lifetime/performance impacts caused by a large amount of reads from our collected data. We will release the collected data to public to encourage future research on this aspect of 3D high-density SSDs.
- The proposed hint commands from applications to SSDs can be successful for the SSDs to reduce the read-induced rewrites, thereby prolonging the SSD lifespan.

Advantages over past work

- Our work quantitatively demonstrates (via our measurement methodology) that the read disturbances become very severe in the state-of-the-art 3D SSDs. In contrast, the previous works [8, 6] only mention the possibly-severe read disturbance

in 2D/3D flash, where the one *cannot* figure out whether such read disturbance actually affects the real usage scenarios.

- We conducted our characterization on 10 different SSDs within at least a half-year period to generate our lifetime-/latency-impact observations. In contrast, the existing flash-disturbance studies [3, 2, 13] performed their characterizations only on a few flash blocks on one or two different types of flashes.

The main challenge of doing such characterization is that we cannot get any meaningful results in the first few weeks since the read disturbance is too small to effect the stored data immediately. We overcome the challenge by our long-term study, where we spent months to collect our targeted data.

6. Why ASPLOS?

Our read latency relaxation proposal focuses on the need to co-design applications and SSDs, which requires the knowledge of both host applications and SSD internals. Hence, this work is suitable for an interdisciplinary system conference, and ASPLOS is such a conference which covers a wide range of system topics, such as storage, operating systems, and compilers.

7. Citation for Most Influential Paper Award

This work extensively characterized multiple state-of-the-art SSDs to quantitatively show the severe read disturbance in the modern 3D flash memories. Motivated by the characterization results, the authors proposed "read latency relaxation", which can reduce the disturbance-induced rewrites to reduce in turn the SSD spent-lifetime without degrading the application-desired performance.

8. Revisions

An earlier version of this work has been submitted before. We addressed the two major concerns and all minor issues. The two major concerns and our changes can be summarized as follow:

- The reviewers indicated that our characterization results with only 4 SSDs (at that time) do not prove that our observations can be generally applied to others brands of 3D SSDs. To address this concern, we extended our characterization to another 6 different 3D SSDs (10 SSDs in total). The newly-collected characterized data show that such lifetime/latency impacts caused by reads can be easily observed by other 3D SSDs as well. As a result, we believe the targeted problem in this paper is quite frequent across high-density 3D SSDs.
- The reviewers believed that our application/SSD co-design proposal cannot perform well on read/write mixed workloads since we only showed the evaluations under read-only workloads (in the earlier submission). To address this concern, we now evaluated our proposal under read/write mixed workloads. The experiments demonstrate that our proposal can achieve similar results to those under the read-only workloads.

References

- [1] Flexible I/O tester. <https://github.com/axboe/fio>.
- [2] Y. Cai, Y. Luo, E. F. Haratsch, K. Mai, and O. Mutlu. Data retention in MLC NAND flash memory: Characterization, optimization, and recovery. In *2015 IEEE 21st International Symposium on High Performance Computer Architecture (HPCA)*, pages 551–563, February 2015.
- [3] Yu Cai, Yixin Luo, Saugata Ghose, and Onur Mutlu. Read disturb errors in MLC NAND flash memory: Characterization, mitigation, and recovery. In *2015 45th Annual IEEE/IFIP International Conference on Dependable Systems and Networks*, pages 438–449. IEEE, 2015.
- [4] Yu Cai, Onur Mutlu, Erich F. Haratsch, and Ken Mai. Program interference in MLC NAND flash memory: Characterization, modeling, and mitigation. In *2013 IEEE 31st International Conference on Computer Design (ICCD)*, pages 123–130. IEEE, 2013.
- [5] Congming Gao, Min Ye, Qiao Li, Chun Jason Xue, Youtao Zhang, Liang Shi, and Jun Yang. Constructing large, durable and fast ssd system via reprogramming 3d tlc flash memory. In *Proceedings of the 52nd Annual IEEE/ACM International Symposium on Microarchitecture*.
- [6] Keonsoo Ha, Jaeyong Jeong, and Jihong Kim. A read-disturb management technique for high-density NAND flash memory. In *Proceedings of the 4th Asia-Pacific Workshop on Systems, APSys '13*, New York, NY, USA, 2013. ACM.
- [7] Huaicheng Li, Mingzhe Hao, Michael Hao Tong, Swaminathan Sundararaman, Matias Björling, and Haryadi S. Gunawi. The CASE of FEMU: Cheap, accurate, scalable and extensible flash emulator. In *16th USENIX Conference on File and Storage Technologies (FAST 18)*. USENIX Association, 2018.
- [8] Chun-Yi Liu, Yu-Ming Chang, and Yuan-Hao Chang. Read leveling for flash storage systems. In *Proceedings of the 8th ACM International Systems and Storage Conference*, 2015.
- [9] Chunyi Liu, Jagadish Kotra, Myoungsoo Jung, and Mahmut Kandemir. PEN: Design and evaluation of partial-erase for 3D NAND-based high density SSDs. In *16th USENIX Conference on File and Storage Technologies (FAST 18)*. USENIX Association, 2018.
- [10] Y. Luo, S. Ghose, Y. Cai, E. F. Haratsch, and O. Mutlu. Heatwatch: Improving 3D NAND flash memory device reliability by exploiting self-recovery and temperature awareness. In *2018 IEEE International Symposium on High Performance Computer Architecture (HPCA)*, Feb 2018.
- [11] Yixin Luo, Saugata Ghose, Yu Cai, Erich F. Haratsch, and Onur Mutlu. Improving 3d nand flash memory lifetime by tolerating early retention loss and process variation. In *Abstracts of the 2018 ACM International Conference on Measurement and Modeling of Computer Systems*.
- [12] Youngseop Shim, Myungsuk Kim, Myoungjun Chun, Jisung Park, Yoona Kim, and Jihong Kim. Exploiting process similarity of 3d flash memory for high performance ssds. In *Proceedings of the 52nd Annual IEEE/ACM International Symposium on Microarchitecture, MICRO '12*, New York, NY, USA. Association for Computing Machinery.
- [13] Qin Xiong, Fei Wu, Zhonghai Lu, Yue Zhu, You Zhou, Yibing Chu, Changsheng Xie, and Ping Huang. Characterizing 3d floating gate NAND flash. In *Proceedings of the 2017 ACM SIGMETRICS / International Conference on Measurement and Modeling of Computer Systems*.